



DATASHEET

JMB585 **PCIe Gen3x2 to 5 SATA 6Gb/s Bridge**

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Revision History

Revision number	Effective date	Description of revision		Author
		Reference	Description of change	
0.1	02/26/2018	-	Draft release.	Steven Lin
0.2	10/05/2018	-	1. Rename JMS585 to JMB585 2. Remove GPIO0 3. Rename Signal Name in 5 Package pin-out 4. Swap PCIe Lane0 and Lane1	MD Lin
1.0	11/01/2018	Chapter 7	Update Electrical characteristics	MD Lin
1.1	12/14/2018	-	Change core power to 1.25V	MD Lin
1.2	05/24/2019	Chapter 7	Updated Power-on sequence	MD Lin
1.3	06/21/2019	Chapter 5	Update Pin Description	MD Lin
2.0	09/15/2019	Figure 2 Chapter 6 Section 6.6	1. Update Application Scenario 2. Change 3.3V to I/O Power Supply, 1.25 V to Core Power Supply in the parameter column 3. Add test environment of power consumption	MD Lin
2.01	01/14/2020	Chapter 5	1. Change PCIe TX capacitor from 200 nF to 220 nF in PCIe Interface Signals 2. Correct GPIO number in LED Indicator 3. 100Mhz -> 100MHz 4. substrate -> Sub-State 5. kΩ -> KΩ	MD Lin

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1 Overview

The JMB585 is a bridge controller between the PCIe host and the storage devices with SATA/AHCI interface. Its upstream port provides a PCIe which data transmission rate for PCIe Gen3x2 specification. Meanwhile, its downstream port can connect to SATA/AHCI storage devices, such as a solid-state drive (SSD). The data speed of each port for the SATA port can arrive at 6Gb/s.

Also, the JMB585 SATA Host provides five ports and supports Port Multiplier (PM). JMB585 supports command-based switching (CBS) and FIS (Frame Information Structure)-based switching (FBS). The default communication method between the SATA Host and the port Multiplier is CBS. FBS allows the Host controller to issue multiple commands that send and receive data simultaneously from any drive.

The JMB585 supports TRIM to the SSD and can transmit and receive data by both of AHCI mode and legacy IDE mode to and from the host respectively.

JMB585 is highly integrated with JMicon PCI Express and SATA self-designed PHYs.

Finally, the JMB585 is a new product that almost reaches PCIe Gen3x2 line bandwidth. JMB585 can be applied on PC. Mobile, servers, IPC, consumer electrical devices, storage device, and NVR/DVR system.

2 Features

2.1 General Features

- 15 GPIOs for customization.
- 25MHz external crystal.
- 76-pin (2 lane PCIe to 5 SATA port) package.
- SPI interface for external SPI Flash (Option ROM).
- Support Windows 7, Windows 10 and Linux-base OS
- Support 3.3V I/O and 1.25V core power.

2.2 PCI Express

- 100 MHz differential PCI Express reference clock in
- Comply with PCI Express Base Specification Revision 3.1a
- Support up to two lanes of PCI Express
- Support PCIe link layer power saving mode.

2.3 SATA

- Comply with SATA Specification Revision 3.2.
- Support 5 SATA ports.
- Support command-based and FIS-based for Port Multiplier.
- Support AHCI mode and IDE programming interface.
- Support Native Command Queue (NCQ).
- Support SATA link power saving mode (partial and slumber)
- Support SATA plug-in detection capable.
- Support drive power control and staggered spin-up.
- Support SATA Partial / Slumber power management state.

3 Block Diagram

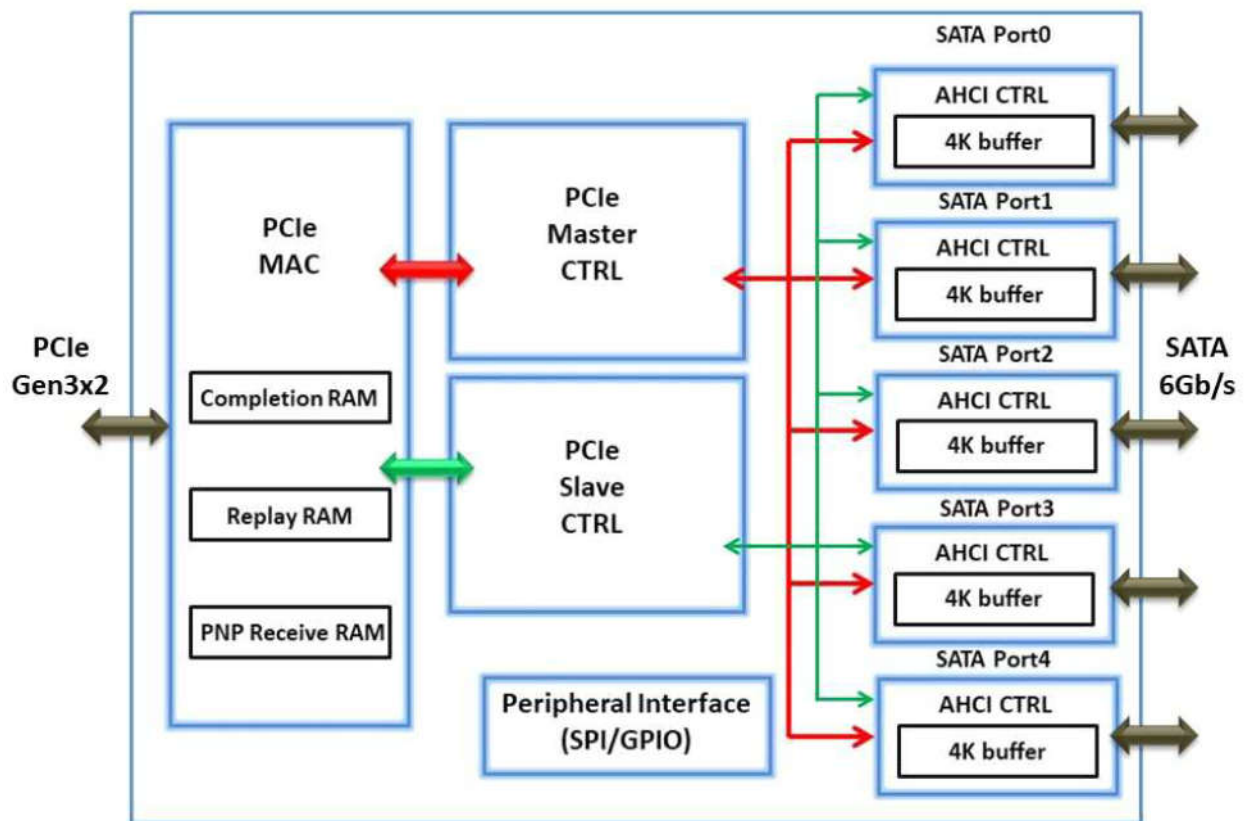
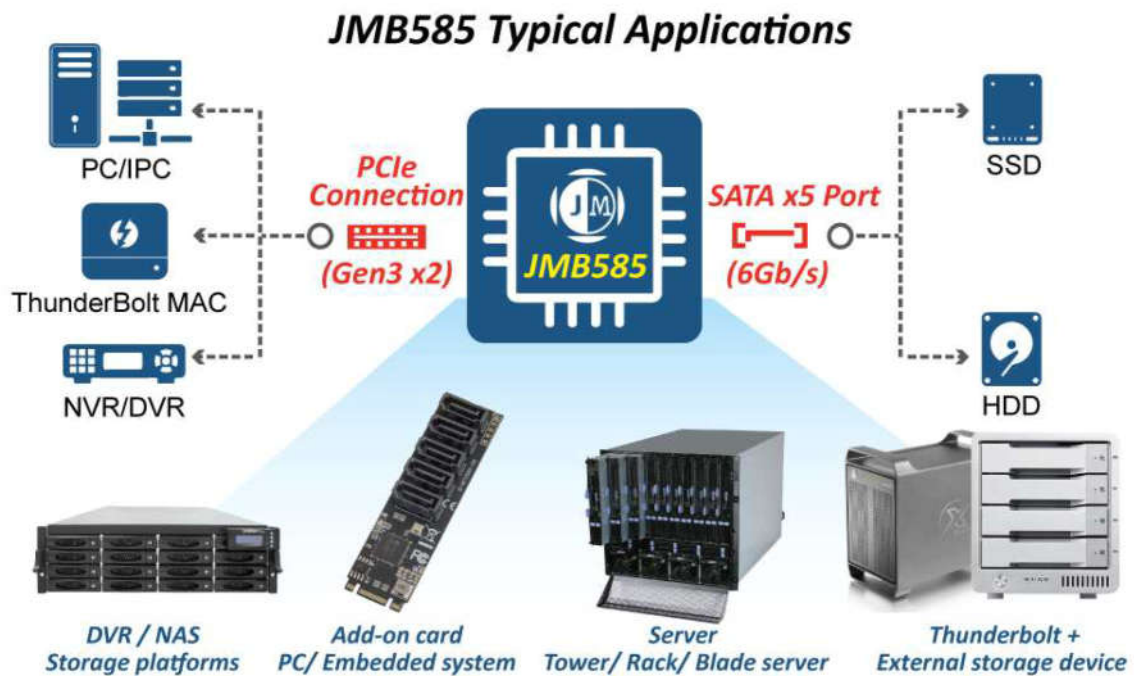


Figure 1 Block Diagram

4 Application



*Reference design, not limited

Figure 2 Application Scenarios

5 Package and Pin Assignments

5.1 Pin Diagram

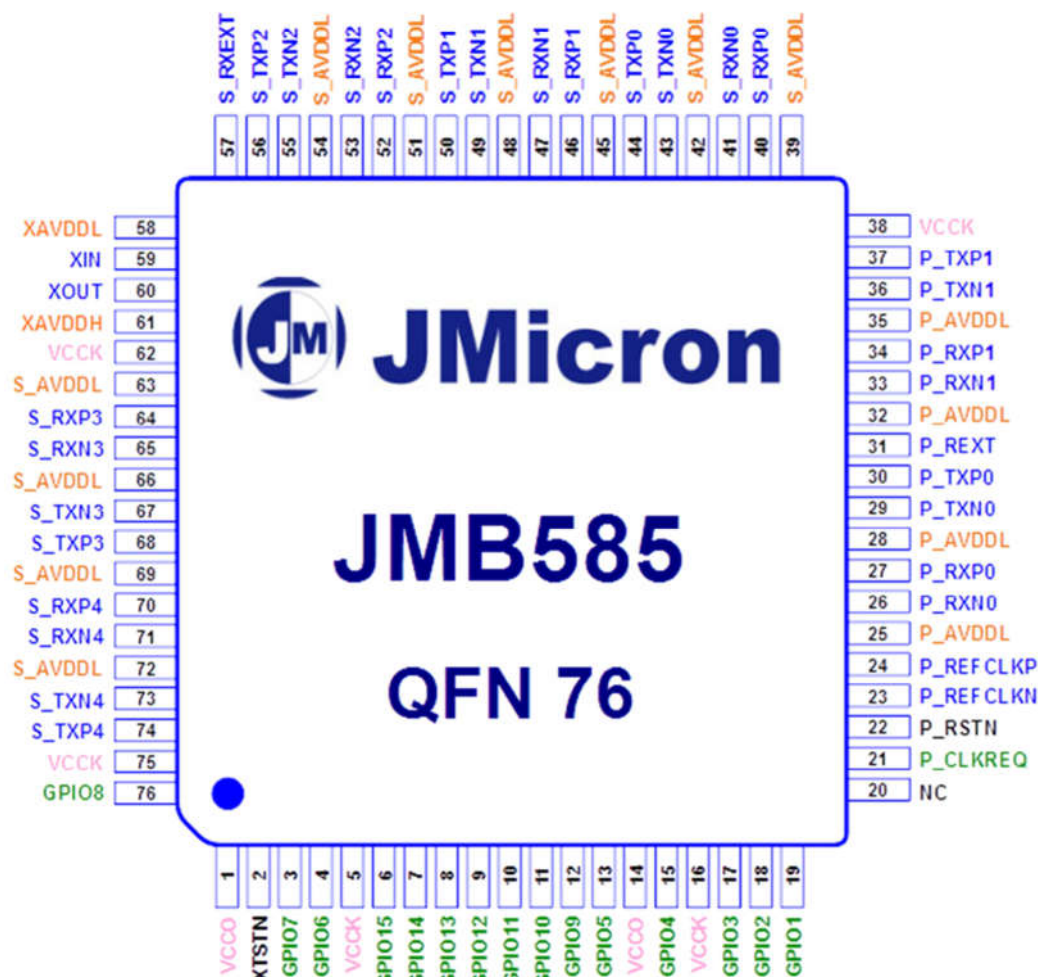


Figure 3 Pin Assignment of JMB585

5.2 Mechanical Dimensions

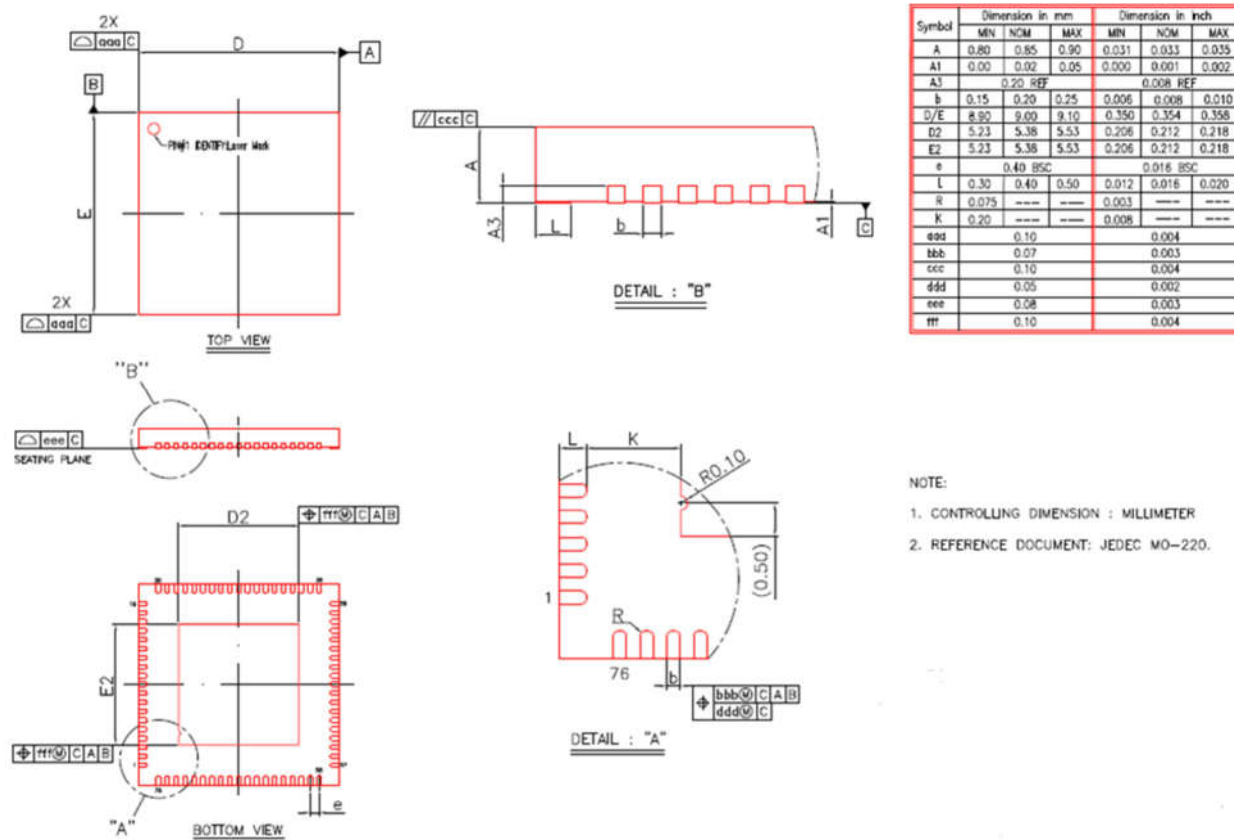


Figure 4 Package Outline Drawing of QFN76 9x9

5.3 Signal Descriptions

5.3.1 Pin Type Definitions

Table 1 Pin Type Definitions

Pin Type	Definitions
A	Analog
D	Digital
P	Power
I	Input
O	Output
IO	Bi-directional
OD	Open-Drain
H	Internal weak pull-high
L	Internal weak pull-low

5.3.2 Pin Descriptions

PCIe Interface Signals

Table 2 PCIe Interface Signals

Signal Name	Pin Number	Type	Description
P_RXN0	26	AI	PCIe Port RX- Signal of Lane 0
P_RXP0	27	AI	PCIe Port RX+ Signal of Lane 0
P_TXN0	29	AO	PCIe Port TX- Signal of Lane 0 A 220 nF capacitor should be connected between this pin and PCIe connector.
P_TXP0	30	AO	PCIe Port TX+ Signal of Lane 0 A 220 nF capacitor should be connected between this pin and PCIe connector.
P_REXT	31	AI	External Reference Resistance A 12K Ω $\pm$ 1% external resistor should be connected to this pin.
P_RXN1	33	AI	PCIe Port RX- Signal of Lane 1
P_RXP1	34	AI	PCIe Port RX+ Signal of Lane 1
P_TXN1	36	AO	PCIe Port TX- Signal of Lane 1 A 220 nF capacitor should be connected between this pin and PCIe connector.
P_TXP1	37	AO	PCIe Port TX+ Signal of Lane 1 A 220 nF capacitor should be connected between this pin and PCIe connector.
P_REFCLKP	24	DI	Differential Clock P 100MHz reference clock from Host.
P_REFCLKN	23	DI	Differential Clock N 100MHz reference clock from Host.
P_RSTN	22	DI	PCIe Reset from Host
P_CLKREQ	21	DIO	This is for L1 Sub-State

SATA Gen3 6Gb/s Interface Signals
Table 3 SATA Gen3 Interface Signals

Signal Name	Pin Number	Type	Description
S_RXP0	40	AI	SATA Port0 RX+ Signal
S_RXN0	41	AI	SATA Port0 RX- Signal
S_TXN0	43	AO	SATA Port0 TX- Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP0	44	AO	SATA Port0 TX+ Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_RXP1	46	AI	SATA Port1 RX+ Signal
S_RXN1	47	AI	SATA Port1 RX- Signal
S_TXN1	49	AO	SATA Port1 TX- Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP1	50	AO	SATA Port1 TX+ Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_RXP2	52	AI	SATA Port2 RX+ Signal
S_RXN2	53	AI	SATA Port2 RX- Signal
S_TXN2	55	AO	SATA Port2 TX- Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP2	56	AO	SATA Port2 TX+ Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_RXP3	64	AI	SATA Port3 RX+ Signal
S_RXN3	65	AI	SATA Port3 RX- Signal
S_TXN3	67	AO	SATA Port3 TX- Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP3	68	AO	SATA Port3 TX+ Signal A 10 nF capacitor should be connected between this pin and SATA connector.

S_RXP4	70	AI	SATA Port4 RX+ Signal
S_RXN4	71	AI	SATA Port4 RX- Signal
S_TXN4	73	AO	SATA Port4 TX- Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_TXP4	74	AO	SATA Port4 TX+ Signal A 10 nF capacitor should be connected between this pin and SATA connector.
S_REXT	57	AI	External Reference Resistance A 12KΩ ±1% external resistor should be connected to this pin.

Crystal Interface

Table 4 Crystal Interface

Signal Name	Pin Number	Type	Description
XIN	59	AI	Crystal Input/ Oscillator Input It is connected to a 25MHz crystal or crystal oscillator. The variation range should be ±30ppm. And the input voltage is 3.3V ±5%.
XOUT	60	AO	Crystal Output It is connected to a crystal. While crystal oscillator is applied, this pin should be reserved for No Connection (NC). The output variation range is around ±30ppm (input dependent). And the input voltage range is 3.3V ±5% (input dependent).

Control and GPIO Interface

Table 5 Control and GPIO Interface

Signal Name	Pin Number	Type	Description
XTSTN	2	DI	MP Test Mode Enable Schmitt trigger input pin. This pin is reserved for IC mass production testing. Keep this pin to logic “1” in normal operation.
GPIO 1	19	DO	SPI SI : SPI Flash SI Pin.
GPIO 2	18	DO	SPI CK : SPI Flash CK Pin.
GPIO 3	17	DO	SPI WP# : SPI Flash WP# Pin.

GPIO 4	15	DI	SPI SO : SPI Flash SO Pin.
GPIO 5	13	DO	SPI CE# : SPI Flash CE# Pin.
GPIO 6	4	DO	SATA0 LED : SATA Port0 PWM (PHY Ready/ Link Busy/ Sleep Dim)
GPIO 7	3	DO	SATA1 LED : SATA Port1 PWM (PHY Ready/ Link Busy/ Sleep Dim)
GPIO 8	76	DO	SATA2 LED : SATA Port2 PWM (PHY Ready/ Link Busy/ Sleep Dim)
GPIO 9	12	DO	SATA3 LED : SATA Port3 PWM (PHY Ready/ Link Busy/ Sleep Dim)
GPIO 10	11	DO	SATA4 LED : SATA Port4 PWM (PHY Ready/ Link Busy/ Sleep Dim)
GPIO 11	10	DO	Disk PWR CTRL: outputs high level when IC has been powered after 5 seconds
GPIO 12	9	DO	Disk PWR CTRL: outputs high level when IC has been powered after 10 seconds
GPIO 13	8	DO	Disk PWR CTRL: outputs high level when IC has been powered after 15 seconds
GPIO 14	7	DO	Disk PWR CTRL: outputs high level when IC has been powered after 20 seconds
GPIO 15	6	DO	Disk PWR CTRL: outputs high level when IC has been powered after 25 seconds

Power Supply Interface

Table 6 Power Supply Interface

Signal Name	Pin Number	Type	Description
VCCO	1, 14	PI	3.3V I/O power supply
VCCK	5, 16, 38, 62, 75	PI	1.25V core power supply
P_AVDDL	25, 28, 32, 35	PI	Analog 1.25V power supply for PCIe
S_AVDDL	39, 42, 45, 48, 51, 54, 63, 66, 69, 72	PI	Analog 1.25V power supply for SATA

XAVDDL	58	PI	Analog 1.25V power supply for crystal oscillator
XAVDDH	61	PI	Analog 3.3V power supply for crystal oscillator

5.4 Function Description

5.4.1 LED Indicator

By default, GPIO 6, 7, 8, 9, and 10 are used as SATA LED indicator. If the user has a different application for LED function, please contact JMicon's AE before PCB layout.

5.4.2 GPIO Initial Value

All GPIOs set as input mode and enable internal pull-up function while in reset.

6 Electrical Specifications

6.1 Absolute Maximum Ratings

Warning: Absolute maximum rating may cause the device permanent damage or reliability will be affected. All voltage is a specified reference to the ground unless otherwise specified.

Table 7 Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units
Digital I/O Power Supply	VCCO _(ABS)	-0.50	-	3.80	V
Digital Core Power Supply	VCCK _(ABS)	-0.50	-	1.38	V
Analog I/O Power Supply	XAVDDH _(ABS)	-0.50	-	3.80	V
Analog Core Power Supply	XAVDDL _(ABS)	-0.50	-	1.38	V
Analog Core Power Supply	S_AVDDL _(ABS)	-0.50	-	1.38	V
Analog Core Power Supply	P_AVDDL _(ABS)	-0.50	-	1.38	V

Digital I/O input voltage	$V_{I(D)}$	-0.50	-	3.80	V
Storage temperature	$T_{STORAGE}$	-40	-	150	°C

6.2 Recommended Operating Voltage and Temperature

Table 8 Operating Voltage and Temperature

Parameter	Symbol	Min	Typical	Max	Units
Digital I/O Power Supply	VCCO	3.00	3.30	3.60	V
Digital Core Power Supply	VCKK	1.20	1.25	1.30	V
Analog I/O Power Supply	XAVDDH	3.00	3.30	3.60	V
Analog Core Power Supply	XAVDDL S_AVDDL P_AVDDL	1.20	1.25	1.30	V
Digital I/O input voltage	$V_{I(D)}$	3.00	3.30	3.60	V
Ambient Operation Temperature	T_A	0	-	70	°C
Maximum Junction Temperature	T_J	-	-	125	°C

Note:

1. All supply mean voltage power noise $\leq \pm 5\%$

6.3 External Clock Source Conditions

Table 9 External Clock Source Conditions

Parameter	Symbol	Min	Typical	Max	Units
External reference clock		-30ppm	25	+30ppm	MHz
Clock Duty Cycle		45	50	55	%

6.4 DC Electrical Characteristics

Table 10 DC Specifications

Parameter	Symbol	Min	Typical	Max	Units
Input low voltage	V_{IL}	-0.3	-	0.8	V
Input high voltage	V_{IH}	2.0	-	3.6	V
Output low voltage	V_{OL}	-	-	0.4	V
Output high voltage	V_{OH}	2.4	-	-	V
Low Level Output Current	I_{OL}	9.8	14.4	19.1	mA
High Level Output Current	I_{OH}	13.9	26.8	45.2	mA

Note:

1. The above test results are under the environment at ambient temperature 25 °C.

6.5 Crystal input

Signal crystal input (25MHz) is needed.

Table 11 Crystal Electrical Specification

Parameter	Symbol	Min	Typical	Max	Units
Crystal Frequency	F_{clk}	-	25	-	MHz
Long term stability (Crystal Only)	$\Delta f_{MAX\_Crystal}$	-30	-	30	ppm

6.6 Power Consumption

The power consumption is tested by the following setting environment and IC condition.

➤ Setting Environment

- Operation System: Windows10 64Bit
- Test tool: PassMark-BurnIn
- Connected device: WD Black 1TB WD1003FZEX, Model:(WD1003FZEX-00K3CA0) *5 Hard Drive Devices

➤ IC Condition

- Device Under Test: Evaluation Board (JMB585-EV-02-01)
- Voltage: 3.3V and 1.25V
- Bin file version: 585v07.Bin
- Device: JMB585

6.6.1 PCIe to SATA

Operation with PCIe L0 state

Table 12 Power Dissipation – Operation with PCIe L0 state

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital I/O Power Supply	VCCO	-	1	-	mA	Operate @ 3.3V Temperature = 25°C
Digital Core Power Supply	VCCK	-	270	-	mA	Operate @ 1.25V Temperature = 25°C
Analog I/O Power Supply	XAVDDH	-	1	-	mA	Operate @ 3.3V Temperature = 25°C
Analog Core Power Supply	XAVDDL	-	18	-	mA	Operate @ 1.25V Temperature = 25°C
Analog Core Power Supply	S_AVDDL	-	600	-	mA	Operate @ 1.25V Temperature = 25°C
Analog Core Power Supply	P_AVDDL	-	300	-	mA	Operate @ 1.25V Temperature = 25°C

Idle with PCIe L0 state
Table 13 Power Dissipation – Idle with PCIe L0 state

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital I/O Power Supply	VCCO	-	1	-	mA	Operate @ 3.3V
Digital Core Power Supply	VCKK	-	250	-	mA	Operate @ 1.25V
Analog I/O Power Supply	XAVDDH	-	1	-	mA	Operate @ 3.3V
Analog Core Power Supply	XAVDDL	-	18	-	mA	Operate @ 1.25V
Analog Core Power Supply	S_AVDDL	-	600	-	mA	Operate @ 1.25V
Analog Core Power Supply	P_AVDDL	-	300	-	mA	Operate @ 1.25V

Suspend with PCIe L2 state
Table 14 Power Dissipation – Suspend with PCIe L2 state

Parameter	Symbol	Min	Typical	Max	Units	Details/ Conditions
Digital I/O Power Supply	VCCO	-	1	-	mA	Operate @ 3.3V
Digital Core Power Supply	VCKK	-	100	-	mA	Operate @ 1.25V
Analog I/O Power Supply	XAVDDH	-	1	-	mA	Operate @ 3.3V
Analog Core Power Supply	XAVDDL	-	18	-	mA	Operate @ 1.25V
Analog Core Power Supply	S_AVDDL	-	330	-	mA	Operate @ 1.25V
Analog Core Power Supply	P_AVDDL	-	190	-	mA	Operate @ 1.25V

6.7 Power-on Sequence

The power-on sequence is defined in Figure 5. Designers should follow all the rules for external power designs.

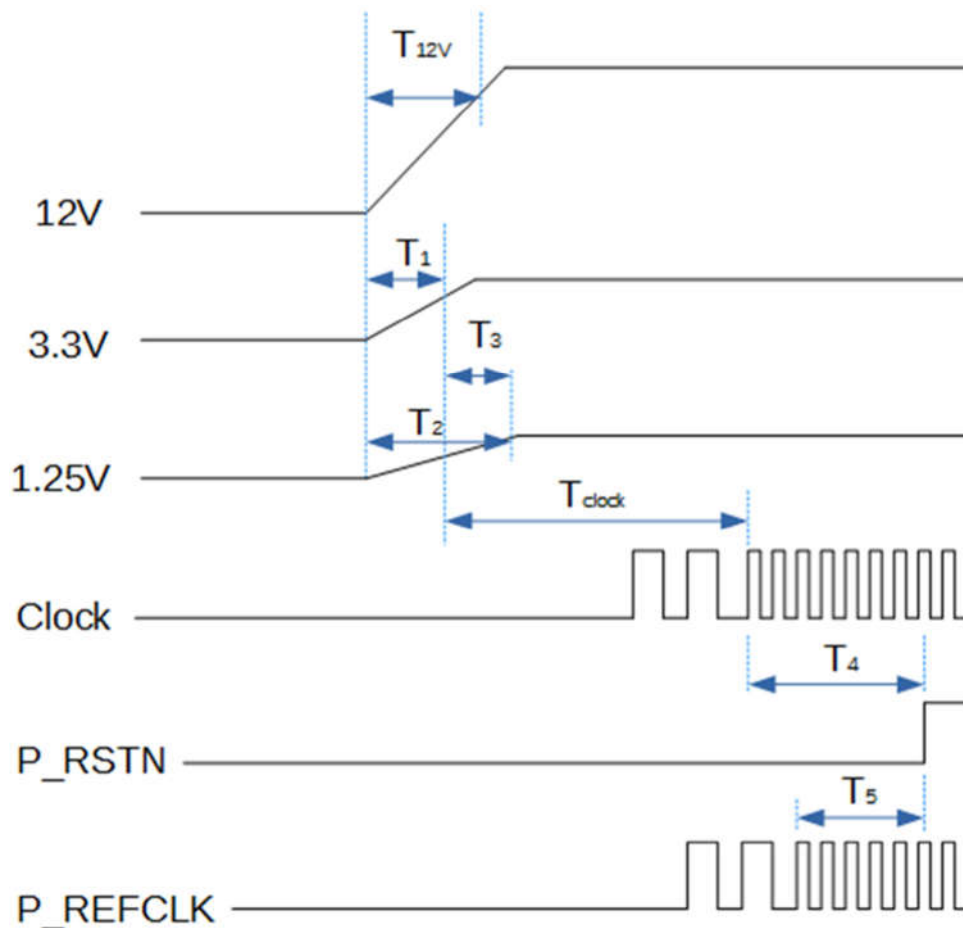


Figure 5 Power-on Sequence

T_{12V}: Rise time for 12V power rail from 10% to 90%

T₁: Rise time for 3V3 power rail from 10% to 90%

T₂: Rise time for 1V25 power rail from 10% to 90%

T₃: Time interval between 3V3 power and 1V25 Power

T_{clock}: Time interval between 3V3 and Stable Clock swing

T₄: Time interval between Stable Clock swing and P_RSTN

T₅: Time interval between Stable P_REFCLK swing and P_RSTN

Note: Clock must meet 25MHz +/-30ppm during the sequence.

The recommended power sequence and timing requirements are listed in Table 15.

Table 15 Power-on timing Requirements

Time	Minimum	Maximum
T _{12V}	-	10ms
T1	-	10ms
T2	-	10ms
T3	-5ms	5ms
T _{Clock}	-	1ms
T4	100ms	-
T5	10ms	-

7 Product Naming Rule

7.1 Format of Part Number

The part number consists of the information of provider, product category, device number, package type, material type, product grade (operating temperature), mask ROM version and device version. The format of the part number is illustrated in Figure 6 below.

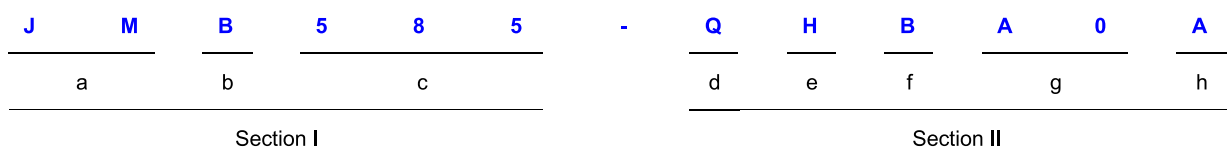


Figure 6 Format of the Part Number

7.2 Explanation of Part Number

Table 16 Explanation of Part Number

Section	Length	Purpose	Code(s)	Meaning
a (JM)	2 digits	Brand name	JM	The provider J Micron
b (B)	1 digit	Product category	B	B = B ridge, S = S oC
c (585)	3 digits	Device number	585	The serial number assigned randomly to form the device name “ JMB585 ” in conjunction with brand name and product category.
d (Q)	1 digit	Package type	B, L, Q, T	B = B GA; L = L QFP; Q = Q FN; T = T QFP
e (H)	1 digit	Material & grade	G, H, I, J	G = Gold wired RoHS compliant halogen-free green product; Ta: 0 ~ 70 °C. H = Copper wired RoHS compliant halogen-free green product; Ta: 0 ~ 70 °C. I = Gold wired RoHS compliant halogen-free green product; Ta: -40 ~ 85 °C. J = Copper wired RoHS compliant

				halogen-free green product; Ta: -40 ~ 85 °C.
f (B)	1 digit	Internal bonding type	A, B, C, ...	A, B, C, ...
g (A0)	2 digit	Version of mask ROM	A0, A1, A2, ... B0, B1, B2, ... Z0	Version A0, A1, A2, ... Version B0, B1, B2, ... Version Z0= no mask ROM
h (A)	1 digit	Version of the IC	A, B, C, ...	Version A, B, C, ...

7.3 Top Mark

Each device has its unique top mark containing the information of provider, device name, part number, manufacturing date code, lot number and pin one identifier for identification. The top mark is illustrated in Figure 7 below.

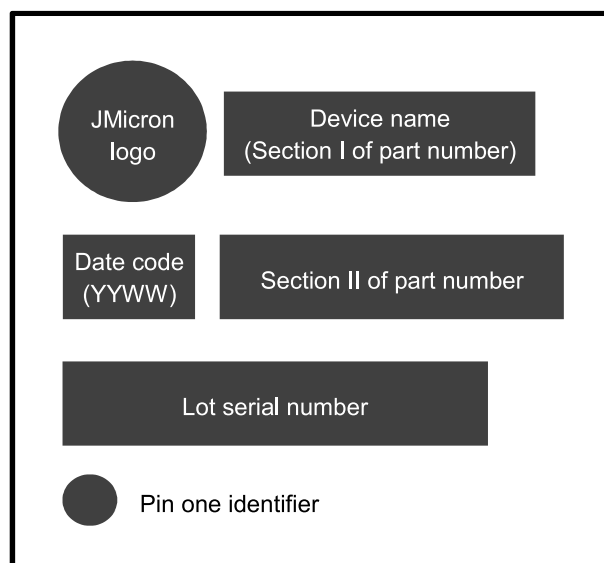


Figure 7 Illustration of Device Top Mark

Note: The above information is only for use in this product datasheet. For more detailed ordering information, please contact to JM micron's Sales Department, representatives, or distributors when ordering parts.

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